Novel Method for Balancing Full Wheatstone Bridge for High-Tolerance Resistive Sensors

Michela Borghetti, *Member, IEEE*, Oscar Casas, *Member, IEEE*, Emilio Sardini, *Member, IEEE*, and Mauro Serpelloni, *Senior Member, IEEE*

***Abstract*—Wheatstone bridge (WB) is widely used in precision measurements involving strain gauges and resistive sensors. However, maintaining balance in a full-bridge configuration becomes increasingly challenging in the presence of high-resistance tolerances—especially in printed electronics, where such variations are common. Traditional compensation methods often entail increased circuit complexity, added cost, and additional sources of error. This article proposes a novel balancing technique for fully resistive WBs, leveraging two voltage References to cancel the output offset even in the presence of resistor tolerances exceeding 0.1%. The method demonstrates robust performance with tolerance levels up to 20%, while preserving high linearity. Simulation results confirm that the approach achieves balanced operation and accurate output even with low-tolerance resistors (1%). Relative to the ideal sensitivity of ($V_{CC}-V_{EE}$), the proposed technique maintains a worst-case sensitivity of 0.8 ($V_{CC}-V_{EE}$), with a theoretically null output offset under balanced conditions. Furthermore, linearity error remains below 0.5% of the full-scale output (FSO), matching the performance of conventional WB circuits affected by mismatch. While the resolution of the voltage references introduces a small, predictable offset—independent of power supply variations—this error is limited to the resolution of the reference itself. Experimental validation using benchtop instrumentation corroborates the simulation findings: with resistors exhibiting 10% tolerance, the maximum deviation between measured and theoretical outputs was 2.4 mV. This deviation remains negligible in terms of estimating fractional resistance changes.**

***Index Terms*—Bridge circuits, electrical resistance measurement, resistive sensors, resistance, resistors, strain measurement.**

I. Introduction

WHEATSTONE bridge (WB) is a circuit configuration extensively used in electrical measurements, and it is a key component in many sensor technologies, ranging from industrial automation [1], [2] systems to biomedical devices [3], [4]. Indeed, WB is especially effective in detecting small changes in resistive sensors. For this reason, WB is extensively used in various applications such as strain gauges, resistance temperature detectors (RTDs), or gas sensors [5]. For example, WB is employed to measure the mechanical stress or strain on materials by detecting small changes in the resistance of piezoresistive sensors [6]. Similarly, in temperature sensing, RTDs in WBs provide highly accurate measurements of resistance as a function of temperature [3]. WB provides accurate measurements in resistance-based sensing applications, and it is commonly used for many reasons: 1) the output of WB is essentially proportional to the reference voltage V_{cc} [7], and this simplifies the estimation of the fractional resistance change of the sensors [5]; 2) the small output of the WB can be easily amplified and filtered with simple and low-cost conditioning circuits [8]; 3) WB is compatible with three-wire or four-wire sensors to compensate the resistance of the long cables; and 4) WB can be adopted in multisensor measurements and power harvesting sensor systems [9].

Despite its widespread use, the implementation of a WB presents several challenges. One of the most critical issues is the accurate balancing of the bridge. In its ideal form, the WB operates with resistances perfectly balanced. When balanced, the bridge produces zero output voltage, enabling the accurate detection of small resistance variations. However, in real-world applications, it is often difficult to achieve perfect balance, particularly in full-bridge configurations, where four resistors must be precisely matched to avoid the initial bias voltage of the bridge [10], [11]. The second challenge involves temperature variations, which affect both sensors and reference resistors and, consequently, the bridge output. To minimize this effect, resistances and resistive sensors with the same temperature coefficient [12] or full-bridge configurations are typically used to compensate for the temperature effects on the four sensors. Any deviation in these resistors can result in measurement errors, compromising the accuracy and reliability of the system. Low-tolerance resistors can be achieved using semiconductor fabrication techniques, which also allow monolithic integration of sensors and conditioning circuits on a single chip. This approach not only reduces parasitic components but also improves precision and stability. For example, in [13], a fully analog, low offset, low noise,

variable gain instrumentation amplifier was proposed to be integrated into a micro-electromechanical systems (MEMSs) accelerometer to compensate for the temperature dependency of sensor sensitivity. Simulations proved that the offset was less than 200 nV, with assuming 10% piezoresistor and CMOS process mismatch. This solution needs the integration of sensors and electronics on the same chip, with unaffordable cost for custom applications.

Printed electronics, such as inkjet printing [14], [15], [16], [17], and aerosol jet printing [18], [19], [20], [21], [22], have gained significant attention in recent years due to their potential for producing flexible, lightweight, and cost-effective electronic devices directly onto flexible substrates. This capability opens up new possibilities in wearable devices, smart textiles, and large-area sensors. However, achieving low-resistance tolerance in WB configurations remains a significant challenge in emerging printed and flexible electronics. Fabrication techniques in these domains often yield resistors with tolerances exceeding 5% [23], primarily due to variability in ink deposition, substrate heterogeneity, and environmental conditions during processing. Such deviations critically impact high-precision applications—such as strain gauges and biosensors—where full-bridge configurations are particularly sensitive to initial resistance mismatches, potentially leading to substantial signal inaccuracies.

To address this issue, several compensation strategies have been explored. Postfabrication trimming techniques, including laser ablation and trace cutting, can substantially improve resistor matching [24], achieving tolerances below 0.02%. However, these methods introduce design complexity and require high-precision instrumentation for accurate control and removal, complicating large-scale or low-cost implementation. Alternatively, the use of adjustable components such as potentiometers offers a practical solution for fine-tuning resistance values [25], [26]. Nonetheless, their adoption is often limited by constraints related to size, mechanical flexibility, and integration within printed or miniaturized systems. Moreover, it is time-consuming and introduces additional sources of error, potentially affecting the long-term stability of resistor values. For example in [26], the offset was reduced from 0.38 mV to 3.8 μV, but it was tested for low-tolerance sensors and the series-parallel-resistor used for the tuning was selected according to the resistance of the sensors. Other more recent approaches are based on the development of self-balancing bridges, which use feedback mechanisms to automatically adjust the resistance values in real time [13], [27], [28], [29]. For example, in [27], a novel approach based on differential measurements of dc currents and bias compensation was proposed for the detection of very small variations of resistors in WB full-bridge configurations. A resolution of 0.00008% with respect to their nominal resistance values and a sensitivity up to 1750 V/% were achieved, but this approach needs active components, which increase costs, dimensions, and complexity. Other similar solutions are limited to quarter-bridge configuration [30], [31], [32], in which the output is affected by temperature changes. Usually, these solutions often rely on ASICs, increasing system cost. Alternative approaches explore advanced materials—such as conductive polymers and nanomaterials—which promise tighter tolerance control during printing, but these solutions are not yet well explored.

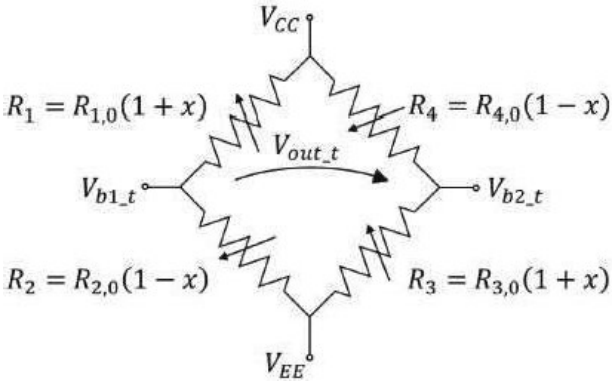


Fig. 1. Traditional full WB circuit. $R_{i,0}$ is the resistance under resting conditions ($x = 0$).

In this context, this work proposes a novel modified full-resistive WB configuration to eliminate the initial offset voltage caused by mismatched resistors, particularly in the context of printed electronics. This novel approach eliminates the need for manual trimming or adjustable resistors while maintaining the accuracy required for precision measurements and complex circuit for the auto-balancing. Through detailed analysis and experimental validation, the effectiveness of this method in achieving balance in a full-bridge configuration is proven, even with resistors with tolerance reached with printed electronics techniques. A comparison with the performance of the traditional WB is presented to define the performance (linearity, uncertainty, and sensitivity) of the proposed solution even in the case of low-tolerance resistors.

II. Proposed Method

A. Traditional WB Method

Fig. 1 shows a traditional full WB circuit for resistive sensors, where

1) R_1, R_2, R_3, and R_4 are the resistances of the four sensors whose value changes according to a physical quantity q (such as heat and stress).
2) $R_{i,0}$ is the nominal nonnull resistance of the ith sensor (at q_0).
3) x is the fractional change in the resistance due to the change of q, defined as $x = ((R_i - R_{i,0})/R_{i,0}) = f(q)$, and thus $|x| \leq 1$.
4) V_{EE} is less than V_{CC} and typically equal to 0 V or $-V_{CC}$.

This configuration is effective in finding q when

$$R_{1,0} = R_{2,0} = R_{3,0} = R_{4,0} = R_0. \tag{1}$$

Under this ideal condition, the relationship between V_{out_t} and x is perfectly linear, as follows:

$$V_{out\_t} = V_{b2\_t} - V_{b1\_t} = x(V_{CC} - V_{EE}) \tag{2}$$

and the gain is $(V_{CC} - V_{EE})$.

However, in practice, sensor fabrication introduces resistance mismatches due to tolerance (denoted as tol, with $0 \leq \text{tol} < 1$), and the ideal condition assumed in (1) is no

longer satisfied. In this case, the output voltage $V_{\text{out\_}t}$ must be reevaluated. The voltages at the intermediate nodes of the WB, V_{b1_t} and V_{b2_t}, can be expressed as follows:

$$V_{b1\_t} = \frac{V_{\text{CC}} \cdot R_{2,0}(1-x) + V_{\text{EE}} \cdot R_{1,0}(1+x)}{\left[R_{1,0}(1+x) + R_{2,0}(1-x)\right]} \tag{3}$$

$$V_{b2\_t} = \frac{V_{\text{CC}} \cdot R_{3,0}(1+x) + V_{\text{EE}} \cdot R_{4,0}(1-x)}{\left[R_{3,0}(1+x) + R_{4,0}(1-x)\right]}. \tag{4}$$

Therefore, the differential output voltage is

$$V_{\text{out}_t} = (V_{\text{CC}} - V_{\text{EE}}) \frac{R_{1,0} \cdot R_{3,0}(1+x)^2 - R_{2,0} \cdot R_{4,0}(1-x)^2}{\left[R_{1,0}(1+x) + R_{2,0}(1-x)\right]\left[R_{3,0}(1+x) + R_{4,0}(1-x)\right]}. \tag{5}$$

This expression depends on seven quantities (x, V_{CC}, V_{EE}, $R_{1,0}$, $R_{2,0}$, $R_{3,0}$, and $R_{4,0}$), which can be reduced to five by introducing two new parameters: α and β. These parameters represent the resistance ratios of the WB when $x = 0$, and are defined as

$$\alpha = \frac{R_{2,0}}{R_{1,0}} \tag{6}$$

$$\beta = \frac{R_{3,0}}{R_{4,0}} \tag{7}$$

where both ratios are positive by definition. Using α and β, (5) becomes

$$V_{\text{out\_}t} = (V_{\text{CC}} - V_{\text{EE}}) \frac{(\beta-\alpha)x^2 + 2(\beta+\alpha)x + (\beta-\alpha)}{\left[(1-\alpha)x + 1 + \alpha\right]\left[(\beta-1)x + 1 + \beta\right]}. \tag{8}$$

This reformulation simplifies the expression of the output voltage and highlights the influence quantities of the bridge configuration. The main issue with this configuration arises when $\alpha \neq \beta$, that is, the resistors are mismatched. In such a case, if $x = 0$, the output is nonzero and equal to

$$V_{\text{out\_}t,x=0} = (V_{\text{CC}} - V_{\text{EE}}) \frac{\beta - \alpha}{(1+\alpha)(1+\beta)}. \tag{9}$$

The more the mismatch between the resistances, the greater this offset. This static offset is problematic, especially because the typical full-scale output (FSO) of the WB is small (often <1 mV) due to small changes of x, and requires amplification. A large offset causes early saturation in the amplification stage, reducing its gain and hence, the resolution of x.

The proposed method aims to null the offset due to the fabrication tolerance of the sensors and to maintain the value of the gain of the bridge to the highest value, which is $(V_{\text{CC}} - V_{\text{EE}})$ in the case of the ideal WB.

B. Proposed Balancing Method: Modified WB Circuit

The proposed circuit, shown in Fig. 2, introduces two voltage references, V_{D1} and V_{D2}, in series to R_2 and R_3, respectively. The intermediate node voltages, V_{b1_n} and V_{b2_n}, become

$$V_{b1\_n} = \frac{V_{\text{CC}} \cdot R_{2,0}(1-x) + (V_{D1} + V_{\text{EE}}) R_{1,0}(1+x)}{R_{1,0}(1+x) + R_{2,0}(1-x)} \tag{10}$$

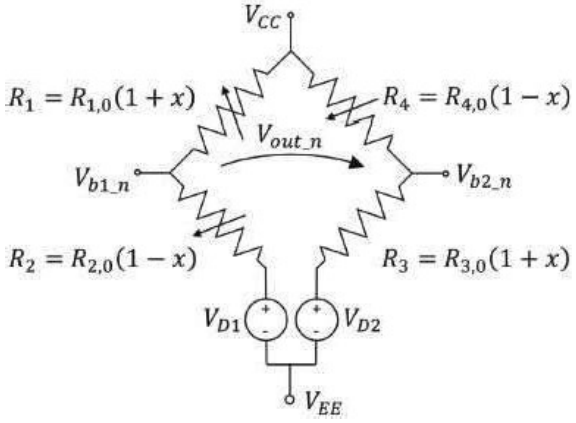


Fig. 2. Modified resistive full WB circuit. $R_{i,0}$ is the resistance under resting conditions ($x = 0$). By properly setting V_{D1} and V_{D2}, $V_{\text{out\_}n}$ is 0 V at $x = 0$.

$$V_{b2\_n} = \frac{V_{\text{CC}} \cdot R_{3,0}(1+x) + (V_{D2} + V_{\text{EE}}) R_{4,0}(1-x)}{R_{3,0}(1+x) + R_{4,0}(1-x)}. \tag{11}$$

Using α and β, they become

$$V_{b1\_n} = \frac{V_{\text{CC}} \cdot \alpha(1-x) + (V_{D1} + V_{\text{EE}})(1+x)}{(1+x) + \alpha(1-x)} \tag{12}$$

$$V_{b2\_n} = \frac{V_{\text{CC}} \cdot \beta(1+x) + (V_{D2} + V_{\text{EE}})(1-x)}{\beta(1+x) + (1-x)}. \tag{13}$$

The main points of a WB are gain, offset, and linearity. In the following, a discussion of how to apply the proposed method is described.

The first operation is performed when x is zero. V_{D1} and V_{D2} are set to V_{D1c} and V_{D2c}, respectively, in order to make $V_{b1\_n} = V_{b2\_n} = V_b$ and thus null the offset at $x = 0$. V_{D1c} and V_{D2c} can be expressed as follows:

$$V_{D1c} = V_b - V_{\text{EE}} + \alpha(V_b - V_{\text{CC}}) \tag{14}$$

$$V_{D2c} = V_b - V_{\text{EE}} + \beta(V_b - V_{\text{CC}}). \tag{15}$$

Based on the value of $V_{b1\_n,x=0}$ and $V_{b2\_n,x=0}$ in the ideal condition, V_b is defined as

$$V_{b\_\text{ideal}} = \frac{(V_{\text{CC}} + V_{\text{EE}})}{2}. \tag{16}$$

In the typical practical implementation of electrical circuits, the power supplies range only between V_{EE} and V_{CC}, and this reduces the allowed range of V_{D1} and V_{D2}. This work considered the abovementioned limitation, and thus Fig. 2 has been redrawn as shown in Fig. 3. Alternative version of the modified resistive full WB circuit, V_{E1} and V_{E2} are defined as

$$V_{D1} = V_{E1} - V_{\text{EE}}, \quad V_{\text{EE}} \leq V_{E1} \leq V_{\text{CC}} \tag{17}$$

$$V_{D2} = V_{E2} - V_{\text{EE}}, \quad V_{\text{EE}} \leq V_{E2} \leq V_{\text{CC}}. \tag{18}$$

Considering the alternative version reported in Fig. 3, as reported for the version of Fig. 2, the first operation of proposed method is to set the value of V_{E1} and V_{E2} when x is 0 in order to make $V_{b1\_n} = V_{b2\_n} = V_b$ and thus null the offset at $x = 0$. The proposed method considers only admissible values for V_{E1} and V_{E2}. Therefore, at $x = 0$, the cases when α or β are greater than 1 cannot be considered, because V_{E1} or V_{E2} are less than V_{EE} to obtain $V_{b1\_n,x=0} = V_{b2\_n,x=0} = V_b$, overcoming their limitation.

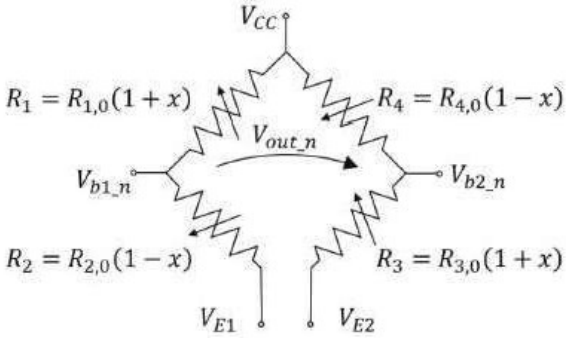


Fig. 3. Alternative version of the modified resistive full WB circuit.

Starting to V_{E1} and V_{E2} range, considering only admissible values and combining (14), (15), (17), and (18), V_b becomes

$$V_b = \frac{(\kappa V_{CC} + V_{EE})}{1+\kappa} \tag{19}$$

where κ assumes different values according to α and β as follows:

$$\kappa = \begin{cases} \alpha; & \alpha \geq \beta \\ \beta; & \alpha < \beta. \end{cases} \tag{20}$$

In this way, the sensitivity of the bridge is maximum.

The balance of the bridge is thus obtained if V_{E1} and V_{E2} assume the values V_{E1c} and V_{E2c}, as follows:

$$V_{E1} = V_{E1c} = \frac{(V_{CC} - V_{EE})(\kappa - \alpha)}{1+\kappa} + V_{EE} \tag{21}$$

$$V_{E2} = V_{E2c} = \frac{(V_{CC} - V_{EE})(\kappa - \beta)}{1+\kappa} + V_{EE}. \tag{22}$$

According to the definition of κ, V_{E1} is equal to V_{EE} when $\alpha \geq \beta$, or V_{E2} is equal to V_{EE} when $\alpha < \beta$.

After rebalancing the bridge with the first operation, the second operation of the proposed method is related to the definition of V_{out_n} in terms of x. Combining (12), (13), (21), and (22), V_{out_n} can be expressed as a function of x, as follows:

$$V_{out\_n} = x\frac{2}{\kappa+1}\frac{(\beta-\alpha)x + (\alpha+\beta+2\alpha\beta)}{[(1-\alpha)x+1+\alpha]\left[(\beta-1)x+1+\beta\right]} \times (V_{CC} - V_{EE}). \tag{23}$$

As expected, if $\alpha = \beta = 1$ (ideal case), this expression is equal to (2). The value of V_{out_n} at $x = 0$ is always null regardless of the values of α and β. Finally, for $|x| \leq 1$, V_{out_n} is between $-(V_{CC} - V_{EE})(1+\beta)/(1+\kappa)$ and $(V_{CC} - V_{EE})(1+\alpha)/(1+\kappa)$.

WB is specially designed for very low values of x ($x \ll 1$). In the case of $x \ll 1$, it is possible to apply the Taylor series limited to the term of the first order to (23) and to obtain a linearization form of V_{out_n}, which is

$$V_{out\_n} \approx V_{out\_n,lin} = x(V_{CC} - V_{EE})\frac{2}{\kappa+1}\frac{(\alpha+\beta+2\alpha\beta)}{(1+\alpha)(1+\beta)} = x(V_{CC} - V_{EE}) \cdot m_{lin}. \tag{24}$$

According to this result, the gain of the bridge is $(V_{CC} - V_{EE})(2/(\kappa+1))((\alpha+\beta+2\alpha\beta)/((1+\alpha)(1+\beta)))$.

Finally, the last operation of the proposed method is to calculate x measuring V_{out_n}. x can be calculated starting from (24) and can be expressed as follows:

$$x_{est,lin} = \frac{V_{out\_n}}{(V_{CC} - V_{EE}) \cdot m_{lin}}. \tag{25}$$

Otherwise, (23) can be rewritten in the form $Ax^2 + Bx + C = 0$ (A, B, C depends on $\alpha, \beta, V_{CC}, V_{EE}$, and V_{out_n}) and x can be exactly found by easily solving the resulting second-order equation.

In Section III, (23) and (24) will be simulated in a MATLAB environment and compared. Results will demonstrate that the approximation error is negligible for $x \ll 1$.

III. Discussion and Simulation Results

In this section, traditional and proposed methods are compared in several scenarios, evaluating their formulas, and comparing numerical results obtained with simulations in a MATLAB environment. To define the possible values assumed by each parameter in real scenarios, strain gauges were considered as the typical sensors that require a WB circuit to measure their resistance change according to the deformation. According to the working conditions of this type of application, the following working conditions were considered.

1) $1 \leq V_{CC} \leq 10$V and $V_{EE} = -V_{CC}$
2) $-5\% \leq x \leq 5\%$ (includes the case of printed strain gauges with high gauge factor).
3) $-20\% \leq$ tol $\leq 20\%$ (thus $(1-\text{tol})/(1+\text{tol}) \leq \alpha \leq (1+\text{tol})/(1-\text{tol})$, and $(1-\text{tol})/(1+\text{tol}) \leq \beta \leq (1+\text{tol})/(1-\text{tol})$), where tol is the expected tolerance of the fabrication process. The boundary conditions for α and β are thus 2/3 and 1.5, respectively. We selected a maximum fabrication tolerance of 20%, considering the resistance tolerance of the sensors fabricated by the emerging printing techniques.

A. Example of V_{out_n} When Tol = ±20%

Aiming at evaluating the behavior of the proposed method in the presence of a real scenario, a high tolerance of 20% for the resistors was adopted. Therefore, as a preliminary study, V_{out_n} was simulated at the boundary conditions of α and β; thus $R_1 = R_3 = R_0 \cdot (1+\text{tol})$ and $R_2 = R_4 = R_0 \cdot (1-\text{tol})$. The following scenario was considered.

1) $\overline{\text{tol}} = \pm 20\%$.
2) $\alpha = 2/3$.
3) $\beta = 1.5$.
4) $V_{CC} = 5$V and $V_{EE} = -5$V.

The curves V_{out_n} obtained by using the proposed method [green line, by applying (23)] and the traditional method [blue line, by applying (8)] are shown in Fig. 4. In the case of the proposed method, V_{out_n} is equal to V_{out_t} in the ideal case ($\alpha = \beta = 1$) (dashed black line) in terms of offset (is null, as expected). V_{E1} and V_{E2} were found to be $-5/3$ and -5 V, respectively.

The dotted red line is the curve obtained by using (24), its linearization form. The gain of V_{out_n} is eight, while it is ten in the ideal case. The proposed method permits compensation of

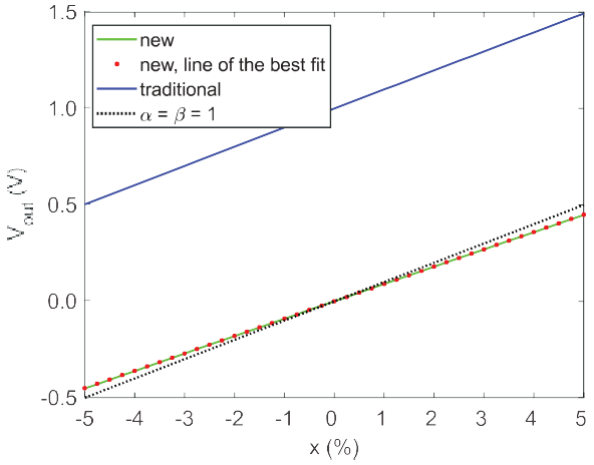


Fig. 4. V_{out} in the case of the proposed method (new) and its linearized form (new, line of the best fit), compared with $V_{out}(x)$ in the case of the traditional configuration (traditional), when $\alpha = 2/3$, $\beta = 1.5$, $V_{EE} = -5$V and $V_{CC} = 5$V. The dashed line is V_{out} when $\alpha = \beta = 1$.

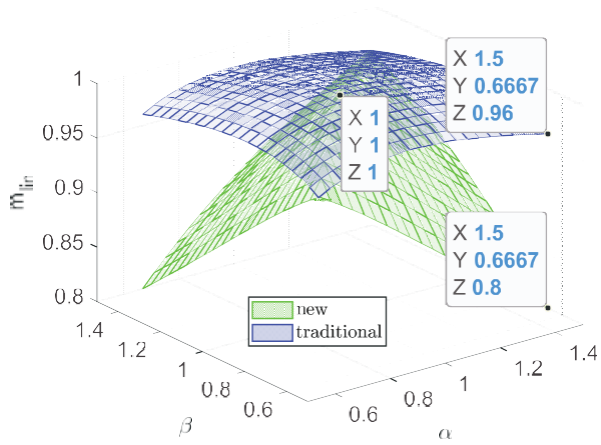


Fig. 5. m_{lin} according to α and β when the proposed method (new) and the traditional configuration (traditional) are used.

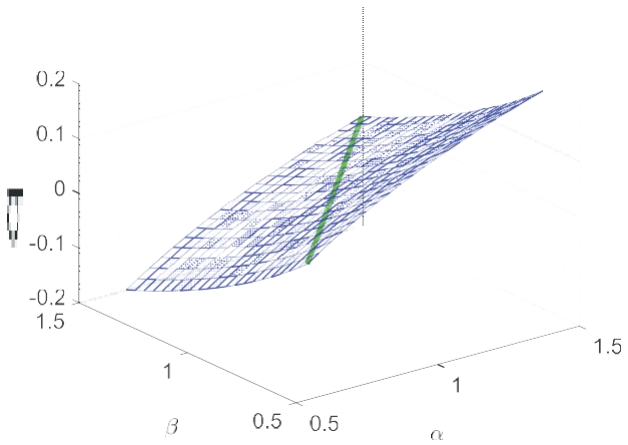


Fig. 6. Traditional circuit offset (expressed as $(V_{out\_t,x=0}/(V_{CC} - V_{EE}))$) according to α and β. The thick line highlights when $q = 0$ V.

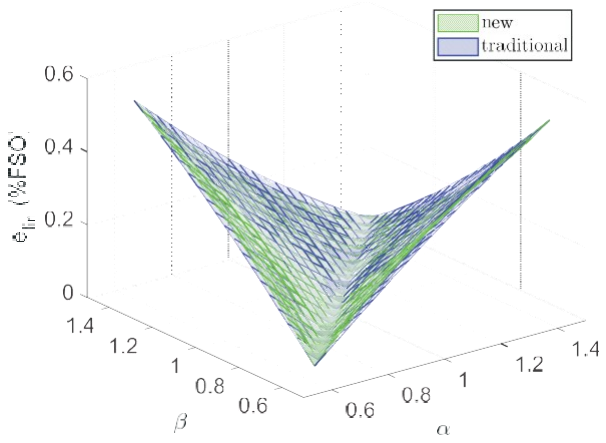


Fig. 7. Linearity error of V_{out_n}, according to α and β in the case of the proposed method (new) and traditional Wheatstone method (traditional).

the high initial offset due to the high tolerance of the resistors without affecting the linearity. The linearity error introduced by the approximated curve is less than 0.5% of FSO. In this case, FSO is 0.8 V. In the nonideal case, in the traditional method, the offset of V_{out_t} is 2 V, and the slope is 9.6.

B. Effects of V_{out} Linearization

Aiming at giving the reader a simplified procedure and an efficient mathematical formulation to use experimentally, the linearization of expression (23) was proposed in Section II. Indeed, $V_{out\_n,lin}$ was proposed to be used to estimate small x and make the estimation easier. As shown in Fig. 5, m_{lin}, defined in accordance with (24) as $(V_{out,lin}/(x(V_{CC} - V_{EE})))$, assumes values from 0.8 to 1 according to α and β values. As expected, m_{lin} is equal to 1 at $\alpha = \beta$. Also in the traditional configuration, V_{out_t} can be approximate with a first-order expression, but the behavior of m_{lin} is different, as follows:

$$m_{lin} = \frac{V_{out\_t,lin}}{(V_{CC} - V_{EE})} = 2\frac{\alpha^2\beta + \alpha\beta^2 + 4\alpha\beta + \alpha + \beta}{(1+\alpha)^2(1+\beta)^2}. \quad (26)$$

m_{lin} is always less than 1, except for the ideal case ($\alpha = \beta = 1$), and it assumes the minimum value of 0.96 at the boundary conditions of α and β.

Regarding the offset $V_{out\_n,lin}$, with the proposed method, the offset is always null, while with the traditional method, the offset is null only when $\alpha = \beta$. Defined $q = (V_{out\_t,x=0}/(V_{CC} - V_{EE}))$, the worst condition for $|q|$ is when $\alpha = (1/\beta) = (1 \pm \text{tol})/(1 \mp \text{tol})$, that is, $R_1 = R_3 = R_0(1 \pm \text{tol})$ and $R_2 = R_4 = R_0(1 \mp \text{tol})$, as shown in Fig. 6.

Finally, the relative linearity error e_{lin} of V_{out_n}, defined as the maximum deviation between V_{out_n} and $V_{out\_n,lin}$ and normalized on FSO, was also found according to α and β values (Fig. 7). The maximum error is obtained at $x = x_{max}$ (or $x = -x_{max}$), when $\alpha \leq \beta$ (or $\alpha > \beta$) and null at $x = 0$ or when $\alpha = \beta$, as also deducted by (23). The results show that the linearity error introduced by the proposed method is not significantly greater than the one introduced by the traditional error, since the behavior is similar to the one obtained with the traditional method. The maximum error is 0.5% FSO: for example, if $V_{CC} = -V_{EE} = 5$ V and $\alpha = (1/\beta) = (2/3)$ (worst condition with tol = 20%), the linearity error is 0.004 mV at $x = 5\%$, and 0.0001 mV at $x = 1\%$.

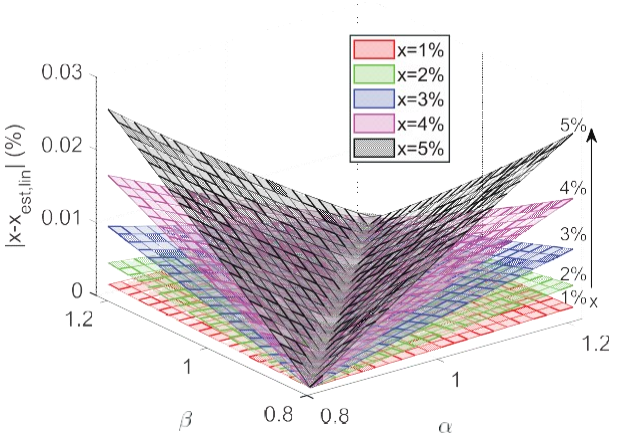


Fig. 8. Linearity error of x, according to α and β in the case of the proposed method.

The linearity error of x according to α and β was shown in Fig. 8 for different x.

In the case of the proposed method, the linearity error of x, defined as $|x - x_{\text{est,lin}}|$, where $x_{\text{est,lin}}$ is the x estimation by using (25), is 0.025% when $x = 5\%$ and 0.002% when $x = 1\%$. From the simulation results, it was also found that the linearity error does not significantly depend on V_{CC} value. Linearity and estimation errors showed a maximum error of 0.5% of FSO in the worst conditions ($\alpha = 1/\beta$ with a 20% tolerance). Simulations revealed that the proposed method introduces similar linearity errors to the traditional method, and the estimation error for x remains very low (e.g., 0.025% at $x = 5\%$). These results demonstrate the effectiveness and accuracy of the proposed approach, even when the linearization form is considered.

C. Gain Setting of the Amplification Stage

As introduced in Section II, the proposed method solves the main issue of the traditional method, that is, the unbalance of the bridge at $x = 0$. Small values of x imply small values of $V_{\text{out\_}t}$ and thus, the need for an amplification stage with high gain (since x is small) to increase the gain of $V_{\text{out\_}t}$. High gain could drive the output of the amplification stage, V_o, to early saturation when the offset $V_{\text{out\_}t,x=0}$ is relevant. To prevent saturation of V_o, in the case of full-scale input of $-x_{\max}$ to $x_{\max}$ and a FSO of $-V_{o,\max}$ to $V_{o,\max}$, the gain of the subsequent amplification stage G should be less than $G_{\max}$, defined as

$$G_{\max} = \frac{V_{o,\max}}{\max\left(|V_{\text{out\_}t}|\right)}. \tag{27}$$

The greater the initial offset, defined as $|V_{\text{out\_}t,x=0}|$, the greater the output $|V_{\text{out\_}t}|$, and thus the smaller G to prevent early saturation. This decrease of G can affect the resolution of the estimation of x. In the worst conditions for the offset (defined in Section III-B), $|V_{\text{out\_}t,x=0}|$ is equal to $\text{tol} \cdot V_{CC}$, and this affects significantly the design of the subsequent amplifying stage. The maximum gain of the amplification stage calculated by using (27) is reported in Table I in the case of the traditional method and the proposed new method, when $\alpha = (1/\beta) = (1 - \text{tol})/(1 + \text{tol})$ and $V_{CC} = 5$V and full-output span for amplification stage is −5 to 5 V). Different conditions of tol and maximum measurable resistance change $x_{\max}$ were considered.

TABLE I

GAIN FOR AMPLIFICATION STAGE USING TRADITIONAL AND NEW METHODS ACCORDING TO TOLERANCE AND MAXIMUM RESISTANCE CHANGE

x_{max} \ $\overline{tol}$	Method	0%	1%	5%	10%	20%
0.1 %	traditional	500	45	10	5	2
	new	500	505	526	556	625
0.5 %	traditional	100	33	9	5	2
	new	100	101	105	111	125
1%	traditional	50	25	8	5	2
	new	50	51	53	56	62
5%	traditional	10	8	5	3	2
	new	10	10	11	11	12

* Conditions: $\alpha = \frac{1}{\beta} = \frac{1-\overline{tol}}{1+\overline{tol}}$, $V_{CC} = 10$V full-output span of -5 V to 5 V.

As shown in the table, the gain of the amplification stage with the proposed new method ensures a maximum gain equal or greater to than the one of the ideal cases (tol = 0%) even when tol = 20%. In the case of the traditional method, when $x_{\max} = 0.1\%$ the gain is 0.34% of the gain found in the ideal case.

D. Consideration About V_{E1} and V_{E2} Resolution

The proposed method is based on the proper regulation of the voltage references V_{E1} and V_{E2} to balance the bridge at $x = 0$. In the case of $V_{E1} = \tilde{V}_{E1}$ (instead of V_{E1c}) and $V_{E2} = \tilde{V}_{E2}$ (instead of V_{E2c}), the actual $V_{\text{out\_}n}$ (called as $V_{\text{out\_}n|\tilde{V}_{E1},\tilde{V}_{E2}}$) could differs from $V_{\text{out\_}n}$ defined in (23). For example, at $x = 0$, $V_{\text{out\_}n|\tilde{V}_{E1},\tilde{V}_{E2}}$ could be nonnull and can be expressed as (28). This offset does not depend on the power supplies

$$V_{\text{out\_}n,x=0|\tilde{V}_{E1},\tilde{V}_{E2}} - \frac{\tilde{V}_{E2} - V_{E2c}}{\beta + 1} - \frac{\tilde{V}_{E1} - V_{E1c}}{\alpha + 1}. \tag{28}$$

The deviation of $V_{\text{out\_}n|\tilde{V}_{E1},\tilde{V}_{E2}}$ from $V_{\text{out\_}n}$ defined in (23) could lead to a wrong estimation of x. The resolution (uV_E) of these voltage references is the one reason for the wrong regulation of V_{E1} and V_{E2}. For this reason, a simulation process was performed considering different values of α, β, V_{CC}, and x and inside the working conditions defined in Section III. Furthermore, it was tested different conditions of uV_E, from 1 μV to 10 mV.

The results showed that the absolute difference between $V_{\text{out\_}n|\tilde{V}_{E1},\tilde{V}_{E2}}$ and $V_{\text{out\_}n}$ defined in (23) is maximum when $V_{E1} = V_{E1c} \mp uV_E$ and $V_{E2} = V_{E2c} \pm uV_E$. Furthermore, fixed V_{E1} and V_{E2}, this difference is maximum when $\alpha = (1/\beta) = \alpha_{\min}$. Finally, fixed V_{E1}, V_{E2}, α, and β, this difference is almost constant (with a variability of less than 0.05%) over the entire range of x. As a representative case, the difference between the estimated x based on $V_{\text{out\_}n|\tilde{V}_{E2},\tilde{V}_{E2}}$ ($x_{\text{estw}uV}$) and the actual x is shown in Fig. 9 according to uV_E and V_{CC} in the case of $x = 0$, $\alpha = 2/3$, $\beta = 1.5$, $V_{E1} = V_{E1c} - uV_E$ and $V_{E2} = V_{E2c} + uV_E$.

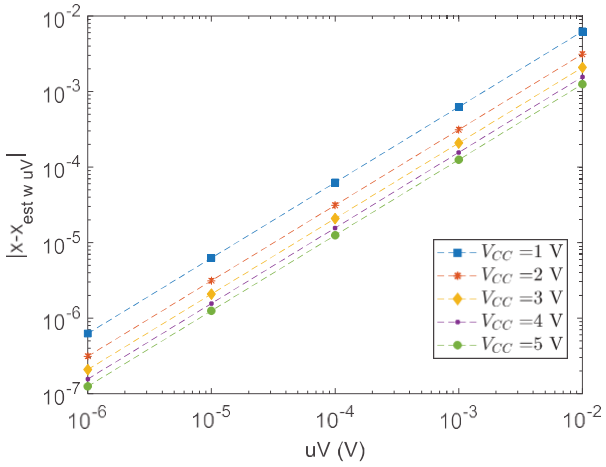


Fig. 9. Differences between x calculated in the ideal case and x_{estwuV} calculated in the case of nonnull resolution of V_{E1} and V_{E2} (uV) when $x = 0$, $V_{EE} = -V_{CC}$ and $\alpha = (1/\beta) = \alpha_{min}$.

The results show that this difference linearly increases according to uV_E and V_{CC}. Indeed, the offset $V_{out\_n,x=0|\tilde{V}_{E2},\tilde{V}_{E2}}$ linearly depends on uV_E.

IV. Experimental Validation

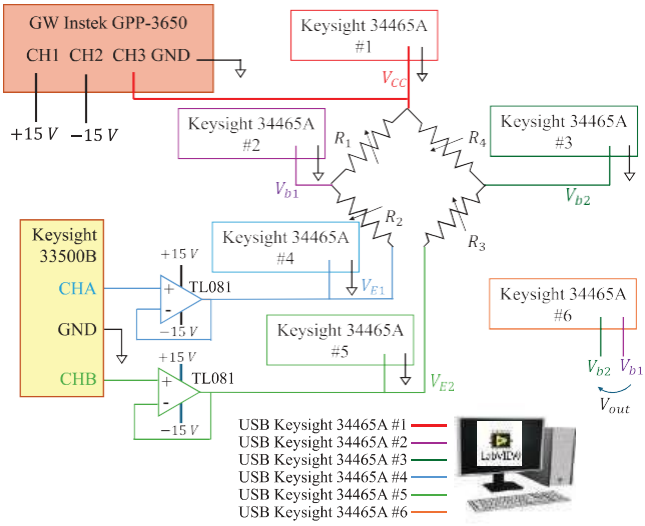
The proposed method was also experimentally evaluated on a full WB with discrete commercial resistors emulating resistive sensors.

A. Experimental Procedure

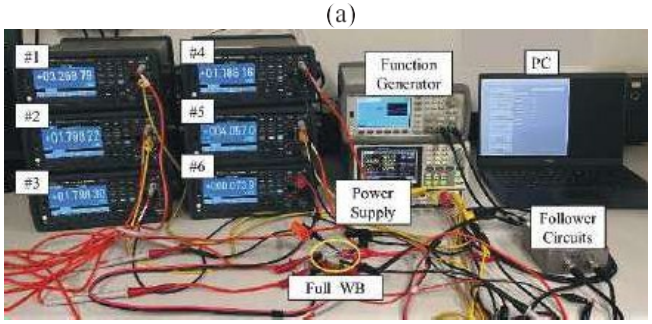
To validate the proposed method, a high-performance instrumentation was adopted. The block diagram and the real experimental setup are shown in Fig. 10(a) and (b).

1) *One GW Instek GPP-3650 Triple-Channel Programmable dc Power Supply:* it provides V_{CC} (for this application was set to 3.255 V) and the double power supply ($\pm$15 V) for the two voltage follower circuits, one devoted to control V_{E1} and the other for V_{E3}. The voltage follower circuits were designed to increase the output impedances of the function generator. V_{EE} is set to 0, and thus no further power supply is needed.
2) *One Keysight 33500B Function Generator:* it provides two independent dc outputs, which are connected to the voltage follower circuit, and used to control V_{E1} and V_{E2}. The accuracy is 2%.
3) Six Keysight 34465A 61/2 digit multimeter for measuring $V_{out\_n}, V_{E1}, V_{E2}, V_{CC}, V_{b1}$, and V_{b2} (according to the voltage values, the declared accuracy is lower than 20 μV for V_{out} and 100 μV for the other voltage quantities, with $k = 2$) and one devoted for resistance measurements (according to the resistance values, the declared accuracy is lower than 38 mΩ, with $k = 2$).

All the instruments were controlled via LabVIEW interfaces. The measurements taken by the six multimeters are triggered via software to ensure the best synchronization: each signal was measured every 300 ms and ten



(a)



(b)

Fig. 10. (a) Experimental setup adopted for the validation of the proposed method. Labels from #1 to #6 indicate multimeters to measure V_{ref}, V_{b1}, V_{b2}, V_{E1}, V_{E2}, and V_{out}, respectively. The power supply provides V_{ref} to the full WB and the power supplies for the follower circuits, while the function generator provides V_{E1} and V_{E2} to the full WB through the follower circuits. Full WB is composed of a network of commercial resistors to obtain R_1, R_2, R_3, and R_4. (b) Schematic of the experimental setup adopted for the validation of the proposed method.

measurements of each signal were visualized and saved every 3 s.

The following method was applied to balance and estimate x.

1) *Estimation of α, β, and κ:* by measuring the resistors in the case of $x = 0$ with a benchtop multimeter, α and β are estimated by using (6)–(7).
2) *Definition of κ and V_b:* κ is defined according to Section II-B and $V_b = (\kappa V_{cc} - V_{cc})/(\kappa + 1)$.
3) *Balance of the Bridge to at $x = 0$:* first, V_{E1} is set to have $V_{b1} = V_b$, and finally, V_{E2} is set to have $V_{b2} = V_b$. V_{E1} and V_{E2} measurements are compared with their theoretical value by applying (21) and (22), respectively.
4) Measurement of V_{out_n}.
5) *Estimation of x via Software:* x was estimated by using (25).

B. Results and Discussion

The modified full WB was built using commercial resistors that simulate the behavior of resistive sensors. Networks of commercial resistors were built to obtain four scenarios of

TABLE II

RESISTANCE VALUES USED FOR VALIDATION TESTS

scenario	*tol*	*x*	R_1	R_2	R_3	R_{14}
1	1% (α =0.98 β =1.02)	0%	1010	990	1010	990
		1%	1020	980	1020	980
		3%	1040	960	1040	960
		5%	1061	941	1061	941
2	5% (α =0.905 β =1.105)	0%	1050	950	1050	950
		1%	1061	941	1061	941
		3%	1082	922	1082	922
		5%	1103	903	1103	903
3	10% (α =0.818 β =1.222)	0%	1100	900	1100	900
		0.5%	1106	896	1106	896
		1%	1111	891	1111	891
		3%	1133	873	1133	873
		5%	1155	855	1155	855
4	5.4% (α =0.905 β =1.035)	0%	1050	950	1025	990
		1%	1061	941	1035	980
		5%	1103	903	1076	940

TABLE III

THEORETICAL AND EXPERIMENTAL V_{out} AND x_{est} VALUES

scenario	x	$V_{out,th}$	$V_{out,meas}$	x_{est}
	%	mV	mV	%
1	0%	0.00	0.65	0.00%
	1%	32.22	32.31	1.00%
	3%	96.67	97.24	3.00%
	5%	161.12	161.13	5.00%
2	0%	0.00	0.29	0.00%
	1%	30.92	29.14	1.00%
	3%	92.76	91.21	3.00%
	5%	154.60	155.69	5.00%
3	0%	0.00	0.54	0.00%
	0.5%	14.65	15.60	0.50%
	1%	29.29	29.88	1.00%
	3%	87.88	88.12	3.00%
	5%	146.47	147.01	5.00%
4	0%	0.00	-0.16	0.00%
	1%	31.46	34.14	1.00%
	5%	157.30	158.10	5.00%

tolerance, shown in Table II: in the first three scenarios, the four resistances were selected to obtain $R_{1,0} = R_{3,0} = 1000(1 + \text{tol})$ and $R_{2,0} = R_{4,0} = 1000(1 - \text{tol})$. Therefore, $\alpha = (1 - \text{tol})/(1 + \text{tol})$ and $\beta = (1 + \text{tol})/(1 - \text{tol})$. In the fourth scenario, four random starting resistances (for the case at $x = 0$) were selected. For each scenario, the resistances were replaced with resistances of value $R_{1,x} = R_{3,x} = R_{1,0}(1 - x)$ and $R_{2,x} = R_{4,x} = R_{2,0}(1 - x)$.

For each x, 20 measurements were taken and averaged. V_{cc} was regulated at (3.25477 $\pm$ 0.00007) V. For each scenario, since β is always greater than α (thus, $\kappa = \beta$), at $x = 0$ V_{E1} and V_{E2} were regulated to obtain V_{b1} and V_{b2} equal to $(V_{cc}(\beta - 1)/(\beta + 1))$.

The expected output $V_{out,th}$ and the measured output $V_{out,meas}$ are reported in Table III. The standard deviation for each point was not represented because it was considered negligible (the standard deviation was always less than 0.005 mV). The difference between the estimated x_{est} and x is negligible, as reported in Table III, as confirmed in Section III with the simulations.

The experimental and theoretical values of V_{E1} and V_{E2} after the balance phase are reported in Table IV, according to

TABLE IV

THEORETICAL (TH) AND EXPERIMENTAL (EXP) V_{E1} AND V_{E2} VALUES IN THE TESTED SCENARIOS

Scenario	V_{CC} (mV)	V_{E1} (mV)		V_{E2} (mV)	
		th	exp	th	exp
1	3254.86	128.91	130.27	0	2.68
2	3254.43	618.78	620.37	0	0.70
3	3254.86	1183.59	1186.01	0	4.14
4	3255.01	417.69	423.72	0	0.57

the scenario. The maximum deviation between the measured and the theoretical values is 2.4 mV. This discrepancy can be justified by considering the accuracy and the resolution of the voltage references, as already confirmed by the simulation results in Section III-D. Furthermore, the mathematical calculation of the theoretical value of V_{E1} and V_{E2} was obtained by the measurements of the resistors, which may further justify the discrepancy. The obtained deviation corresponds to the resolution of an analog-to-digital converter powered between −3.3 and 3.3 V with an 11.4-bit resolution. This difference does not contribute to the deviation of the calculated x from the expected one, even considering the linearized form and this contributes to proving the effectiveness of the proposed method for estimate x.

V. CONCLUSION

This study introduces a modified full WB architecture that incorporates only two additional voltage reference components to effectively suppress output offset arising from resistance mismatches. In contrast to conventional trimming or calibration methods, the proposed technique eliminates the need for sensor redesign, postfabrication tuning, or the integration of costly active components such as custom integrated circuits. This approach is particularly advantageous for high-tolerance printed resistive sensors, where conventional compensation methods often result in substantial offset errors.

In such scenarios, uncalibrated mismatches can drive the amplifier into saturation, thereby reducing the usable dynamic range and rendering the system gain more sensitive to initial mismatches than to the sensor's full-scale response. The proposed method circumvents this issue by statically balancing the bridge prior to operation—that is, under unloaded sensor conditions—ensuring a zero-offset starting point. This enables the amplification stage to operate at higher gain settings, thereby enhancing resolution without compromising system linearity.

Empirical and simulation-based evaluations demonstrate that the technique sustains a linearity error below 0.5% of the FSO, even under resistor tolerances of up to 20%. Moreover, the approach retains high accuracy and linearity with low-tolerance resistors (e.g., 1%). However, its performance is inherently influenced by the resolution, stability, and accuracy of the voltage references. Although the power supply stability requirements remain comparable to those of conventional WB circuits, the finite resolution of the voltage references may introduce a minor output

offset—bounded by the reference resolution in the worst-case scenario.

Future developments will focus on the implementation of this compensation strategy in practical systems, particularly in printed resistive sensor networks, and its integration with cost-effective embedded electronics platforms.

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